CLAIMS

What is claimed is:

1. A computer system, comprising:

a central processing unit ("CPU");

a bridge device coupled to a main memory;

a cache controller coupled between the bridge device and the CPU; and

a cache memory coupled to the cache controller and providing cache memory space to the CPU;

wherein the cache controller allows communication between the CPU and the bridge device when the CPU communicates using a first communication protocol and the bridge device communicates using a second communication protocol, and wherein the cache controller allows communication between the CPU and the bridge device when the CPU communicates using the second communication protocol and the bridge device communicates using the first communication protocol.

2. The computer system of claim 1 wherein the cache controller comprises switch logic coupled between a first protocol interface and a second protocol interface, the switch logic implements a communication protocol to transfer information between the first protocol interface and the second protocol interface.

3. The computer system of claim 2 wherein the communication protocol implemented by the switch logic is different from the first and second communication protocols.

4. The computer system of claim 3 wherein the cache controller further comprises a cache memory interface coupled to the cache memory, the cache memory interface is operable to access data stored in the cache memory according to address information provided to the cache controller.

5. A cache controller, comprising:

a first interface operable to communicate to an external device using a first communication protocol;

a second interface operable to communicate to an external device using a second communication protocol different than the first communication protocol; and

a cache memory interface coupled to the first and second interfaces, the cache memory interface controls reading and writing to a cache memory;

wherein the first interface selectively communicates to an external device being one of a CPU and a bridge device;

wherein the second interface selectively communicates to an external device being one of a CPU and a bridge device.

6. The cache controller of claim 5 further comprising a control module coupled to the first and second ports, the control module is operable to receive a control signal to select that the first interface communicate to one of the CPU and the bridge device.

7. The cache controller of claim 6 wherein the control module is operable to receive a control signal to select that the second interface communicate to one of the CPU and the bridge device.

8. The cache controller of claim 5 wherein the cache memory interface determines whether address information from a CPU matches address tags in a tag memory.

9. The cache controller of claim 8 wherein, if the address information matches an address tag, the cache controller provides data from the cache memory to the requesting CPU.

10. The cache controller of claim 8 wherein, if the address information does not match an address tag, the cache memory interface creates a new address tag and designates a memory location in a cache memory to store data associated with the address information.

11. The cache controller of claim 8 wherein, if the address information does not match an address tag, the cache controller forwards the address information to a bridge device coupled to one of the first port and the second port.

12. A method, comprising:

configuring a first port of a cache controller to communicate to an external device, wherein the first port selectively communicates to one of a CPU and a bridge device using a first communication protocol; and

configuring a second port of the cache controller to communicate to an external device, wherein the second port selectively communicates to one of a CPU and a bridge device using a second communication protocol.

13. The method of claim 12 further comprising one of:

configuring the first interface to communicate to a CPU and configuring the second interface to communicate to a bridge device; and

configuring the first interface to communicate to a bridge device and configuring the second interface to communicate to a CPU.

14. The method of claim 12 further comprising accessing data in a cache memory and transmitting data to a requesting CPU if address information of a CPU request matches an address tag stored by the cache controller.

15. The method of claim 12 further comprising creating an address tag and designating a location in a cache memory to store data associated with address information of a CPU request if the address information does not match address tags stored by the cache controller.

16. A computer system, comprising:

a central processing unit ("CPU");

a bridge device coupled to a main memory; and

means for reading and writing to a cache memory coupled between the CPU and the bridge device;

wherein said means for reading and writing to the cache memory allows communication between the CPU and the bridge device when the CPU communicates using a first communication protocol and the bridge device communicates using a second communication protocol, and allows communication between the CPU and the bridge device when the CPU communicates using the second communication protocol and the bridge device communicates using the first communication protocol

17. The computer system of claim 16 further comprising means for determining whether address information from a CPU request matches an address tag stored in the cache controller.

18. The computer system of claim 17 further comprising means for accessing data stored in the cache memory if the address information matches an address tag.

19. The computer system of claim 17 further comprising means for creating a new address tag for association with the address information and designating a memory location in the cache memory for storing data associated with the address information if the address information does not match an address tag.

20. A cache controller, comprising:

a plurality of first communication protocol interfaces that allow communication between the cache controller and at least one of a processor and a bridge device , wherein each of the processor and

bridge device communicates using a first communication protocol; and

a plurality of second communication protocol interfaces that allow communication between the cache controller and at least one of a processor and a bridge device, wherein each of the processor and bridge device communicates using a second communication protocol.

21. The cache controller as defined in claim 20 wherein the cache controller allows communication between the CPU and the bridge device when the CPU and the bridge device communicate using a first communication protocol, wherein the cache controller allows communication between the CPU and the bridge device when the CPU and the bridge device communicate using a second communication protocol, wherein the cache controller allows communication between the CPU and the bridge device when the CPU communicates using the first communication protocol and the bridge device communicates using the second communication protocol, and wherein the cache controller allows communication between the CPU and the bridge device when the CPU communication using the second communication protocol and the bridge device communicates using the first communication protocol.

22. The computer system of claim 20 wherein the cache controller comprises a control unit coupled to the plurality of ports, the control unit operable to configure the ports according to a control signal such that the cache controller allows one of:

communication between the CPU and the bridge device when the CPU and the bridge device communicate using a first communication protocol;

communication between the CPU and the bridge device when the CPU and the bridge device communicate using a second communication protocol;

communication between the CPU and the bridge device when the CPU communicates using the first communication protocol and the bridge device communicates using the second communication protocol; and

communication between the CPU and the bridge device when the CPU communication using the second communication protocol and the bridge device communicates using the first communication protocol.

23. A computer system, comprising:

a central processing unit ("CPU");

a bridge device coupled to a main memory;

a cache controller coupled between the bridge device and the CPU; and

a cache memory coupled to the cache controller and providing cache memory space to the CPU;

wherein the cache controller allows communication between the CPU and the bridge device when the CPU and the bridge device communicate using different communication protocols, and wherein the cache controller also allows communication between the CPU and the bridge device when the communication protocols of the CPU and bridge device are reversed.

24. A computer system, comprising:

a processor having an associated communications protocol;

a bridge device having an associated communications protocol;

a cache controller comprising

a plurality of first communication protocol interfaces each allowing communication using an individual one of a plurality of communication protocols;

a plurality of second communication protocol interfaces each allowing communication using an individual one of a plurality of communication protocols; and

wherein the cache controller couples the processor and the bridge device.

25 The computer system as defined in claim 24 wherein each of the processor and the bridge device are coupled to the plurality of first communication protocol interfaces.

26. The computer system as defined in claim 24 wherein each of the processor and the bridge device are coupled to the plurality of second communication protocol interfaces.

27. The computer system as defined in claim 24 wherein the processor is coupled to one of the first communication protocol interfaces, and the bridge device is coupled to one of the second communication protocol interfaces.

28. The computer system as defined in claim 24 wherein each of the processor and the bridge device are coupled to the plurality of second communication protocol interfaces.